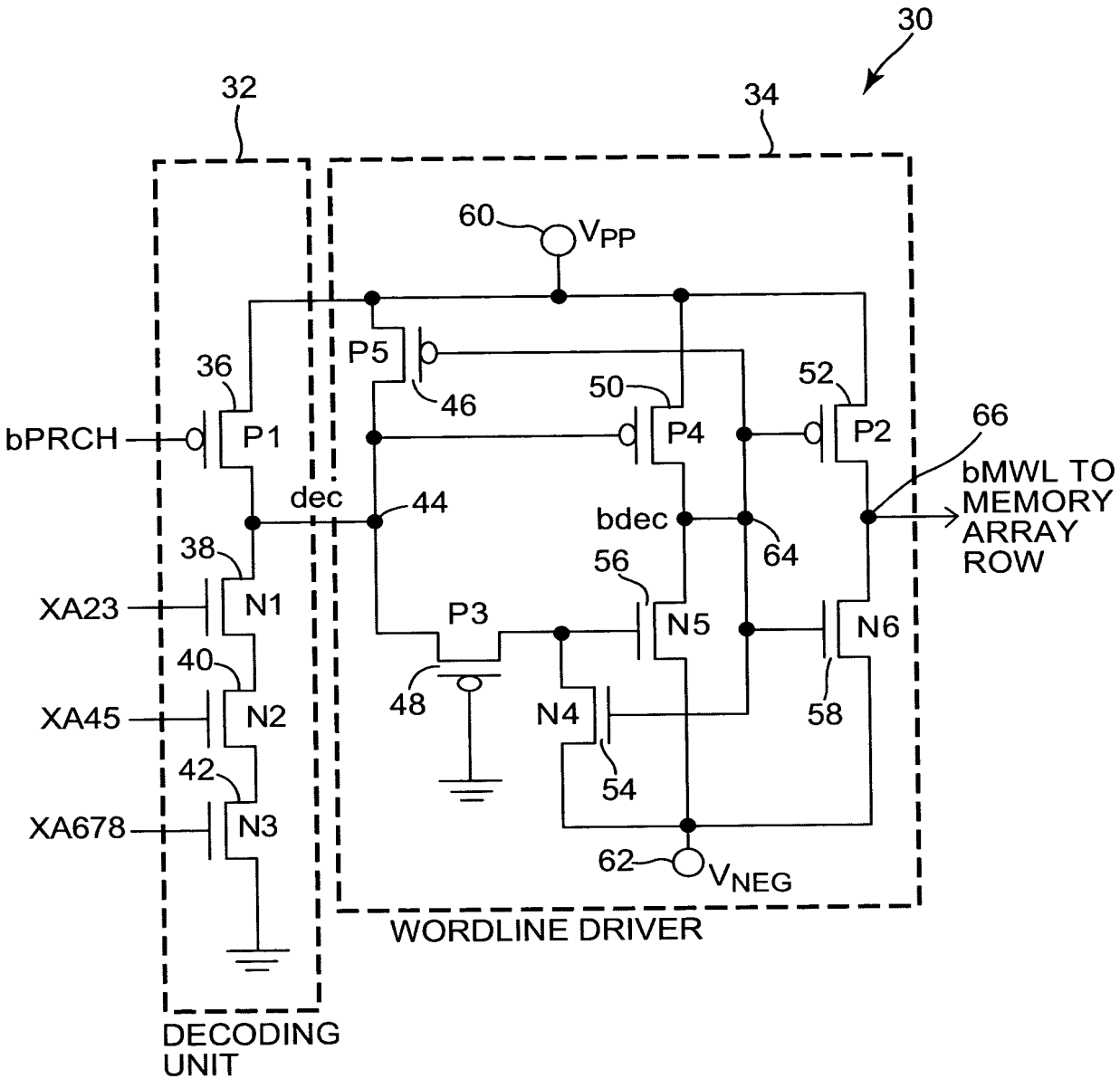

Fig. 1
PRIOR ART

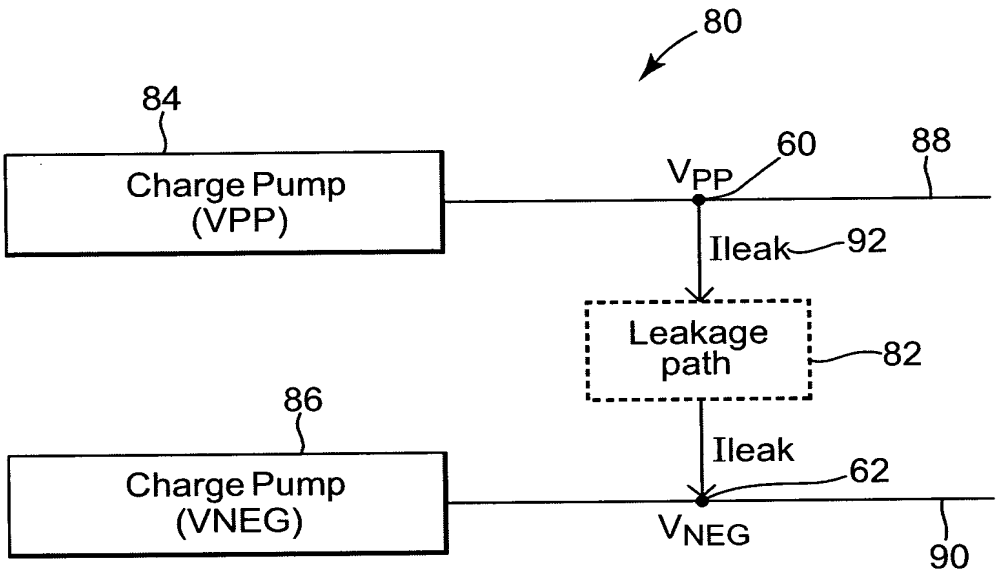

Fig. 2
PRIOR ART

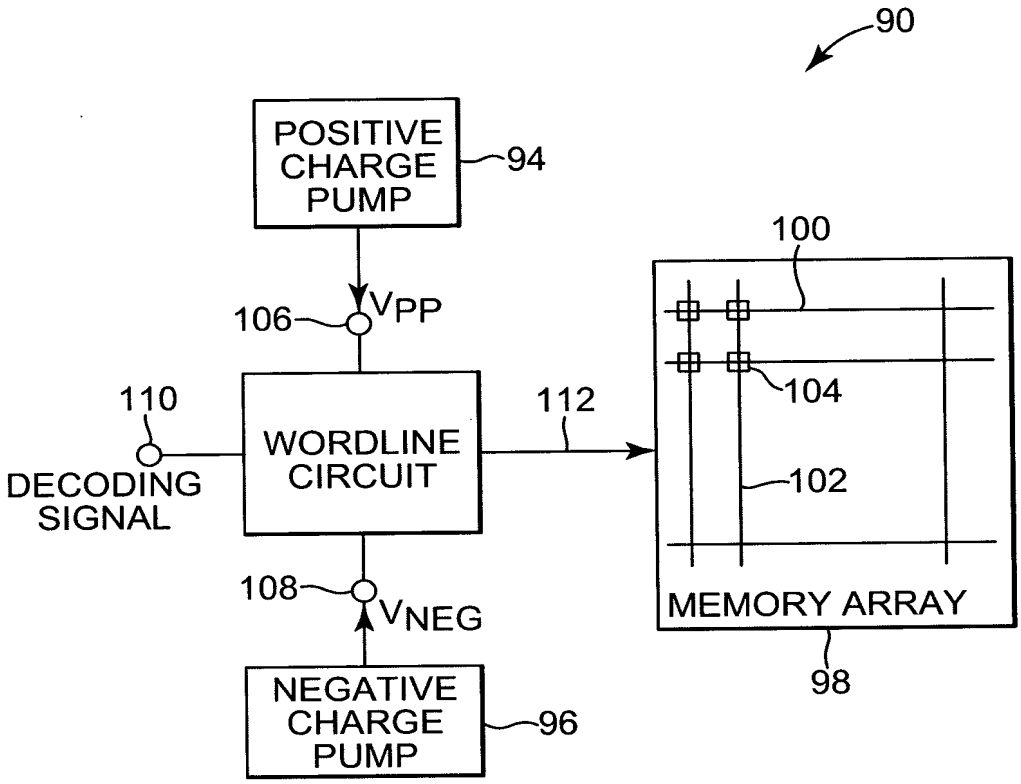
90
POSITIVE CHARGE PUMP
94
100
106
VPP
110
DECODING SIGNAL
WORDLINE CIRCUIT
112
104
102
MEMORY ARRAY
98
108
VNEG
NEGATIVE CHARGE PUMP
96

Fig. 3

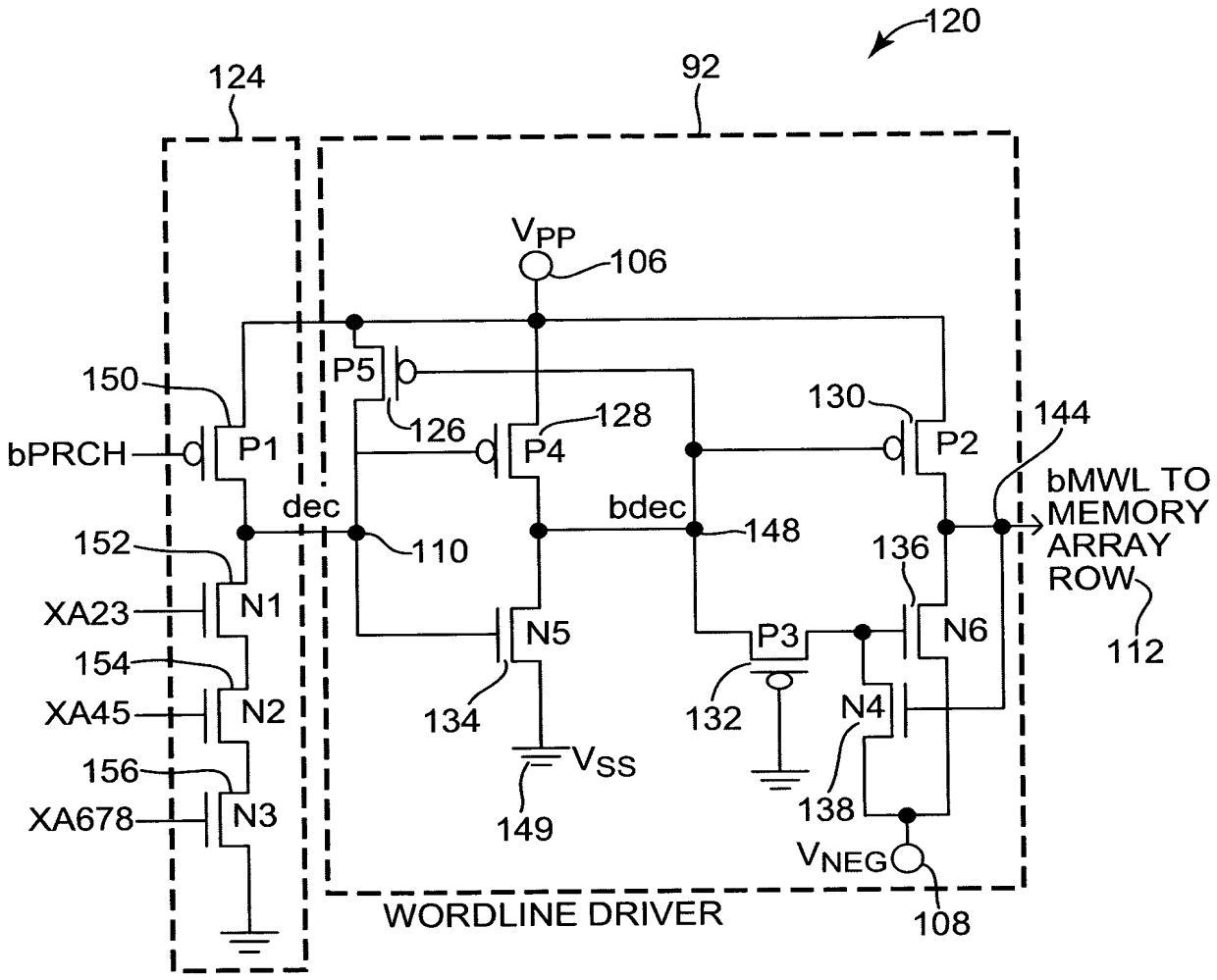
120
124
92
V_{PP}
106
150
P5
126
128
130
144
bPRCH
P1
P4
P2
bMWL TO MEMORY ARRAY ROW
dec
bdec
152
110
148
136
XA23
N1
N5
P3
N6
112
154
XA45
N2
134
132
N4
156
V_{SS}
138
XA678
N3
149
V_{NEG}
WORDLINE DRIVER
108

Fig. 4